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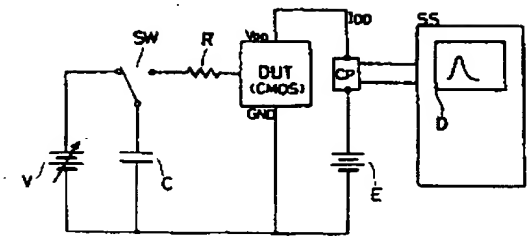
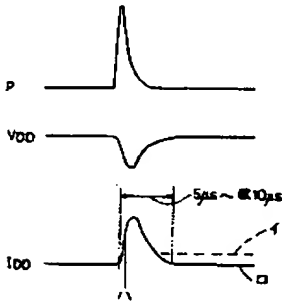
TITLE : MEASUREMENT FOR LATCH UP PHENOMENON OF CMOS ELEMENT





ABSTRACT : PURPOSE: To enable accurate measurement of latch up phenomenon without delay in the response, the displaying an output current waveform on a synchroscopic screen at the time when an electrostatic pulse is applied to an input terminal of a CMOS element.

CONSTITUTION: An electrostatic pulse is applied to an input terminal of a device DUT of a CMOS element and the resulting output current waveform is displayed on a synchroscope SS through a current probe CP. The waveform at the transi tion of current IDD pulses for about 5~ several ten μsec when a latch up of the device DUT takes place. Then, when the current limiting capacity of the power source E is large, after the latch up thereof, a relatively large current flows as shown by the broken line (a) while no large current flows after the latch up as shown by the solid line (b) when it is small. Then, when the current limiting capacity of the power source E is large, the breakdown of the device DUT by separating the power source E from the circuit immediately after the observation of the pulse waveform. While no latch up takes place, such a pulsing current will not flow. Thus, judgement on the presence of latchup phenomenon can be done depending on the waveform on the screen of the synchroscope SS.